UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,898	10/01/1998	JAMES AKIYAMA	42390.P3373	7208

7590 11/21/2001

JAMES H SALTER
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/164,898	Aklyama, James
Examiner	**Art Unit**
Pierre Vital	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 9, 2001*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *19-37* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *19-37* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Request for Continued Examination

1. The request filed on October 9. 2001 for a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 based on parent Application No. 09/164,898 is acceptable and a RCE has been established. An action on the RCE follows.

Response to Amendment

2. This Office Action is in response to applicant's communication filed October 9, 2001 in response to PTO Office Action dated June 25, 2001. The applicant's remarks and amendment to the specification and/or the claims were considered with the results that follow.

3. Claims 19-37 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. Claims 1-3 and 7-18 have been canceled. Claims 19-37 have been added. As a result, claims 19-37 are now pending in this application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 19-22, 24-31 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723).

As per claims 19, 25, 28 and 35, Anderson teaches a system for multi-threaded disk drive interrupt processing wherein the first and second disk drives 110 and 112 may be integrated device electronics (IDE) disk drives wherein the disk drive itself contains many of the required interface components; with IDE disk drives, a single interface coupled to the bus system 108 is capable of operating multiple IDE disk drives [Col.5, lines 28-33]; it is the instructions in the BIOS 106 itself that controls the positioning of the read/write head in the first disk drive 110 and the second disk drive 112 [Col.8, lines 12-15]; in the disk striping embodiment of the system 100, a data file is apportioned into blocks that are alternately stored (interleaved) on the first drive 110 and the second drive 112; the system 100 advantageously allows the BIOS 106 to issue commands to both the first disk drive 110 and the second disk drive 112 to allow each of the first and second disk drives to simultaneously (parallel) perform the consuming task of positioning the read/write head at the proper location on the disk drive [Col.8, lines 62-67; Col.9, lines 1-3]; with respect to the disk striping aspect of the system 100, the operating system behaves if there is a

single disk drive (single physical drive) rather than the first disk drive 110 and the second disk drive 112 [Col.7, lines 60-63]. However, Anderson fails to specifically teach an interface connected to the system bus and communicating with the BIOS; and a striping controller connected between said first and second disk drives and said interface, said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel.

Jones discloses an interface connected to the system bus and communicating directly with the BIOS [Col.14, Lines 24-31; col.23, lines 15-25]; a striping controller connected between said first and second disk drives and said interface [Col.14, Lines 28-33], said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel [Col.16, Lines 32-35].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones before him at the time the invention was made, to modify the system taught by Anderson to include a controller for controlling striping of the disks, the controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel because it would have improved system performance by allowing reconstruction of data without any down time as taught by Jones.

As per claims 20, 29 and 36, Anderson teaches interleaving data so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive [col.4, lines 16-30].

As per claims 21 and 30, Anderson discloses data being transmitted between the system bus and the first and second disk drives is subdivided into a plurality of sequential blocks [col.8, lines 62-65].

As per claims 22 and 31, Anderson teaches the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks [col.11, lines 35-50; col.12, lines 3-23].

As per claim 34, Anderson discloses a control logic receives a system request intended for a single physical drive from the system bus [Col.7, lines 60-63].

As per claims 24 and 33, Anderson discloses mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive [Col.8, lines 54-61].

As per claim 26, Anderson discloses receiving an IDE request at a striping controller [col.8, lines 65-67].

6. Claims 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723) and further in view of Jenkins (US4,047,157).

As per claims 23 and 32, the combination of Anderson and Jones teach the claimed invention as detailed above in the previous paragraphs. However, neither Anderson nor Jones

specifically teach that the system request includes a sector bit string, a head bit string, a track bit string and a driver bit as recited in the claims.

Jenkins teaches a controller for use in a data processing system wherein in the track/sector register 146 Track Address and Sector Address bit positions identify, respectively, the track and sector on a disk to be involved in a transfer; in a fixed-head unit, the Track Address bits identify a specific head [Col.20, lines 38-42]; a Write signal, produced in response to the function bits, enables drivers 297 to load data onto the data set 101 [Col.26, lines 26-28].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones and Jenkins before him at the time the invention was made, to modify the system taught by Anderson and Jones to include sector bit string, head bit string, track bit string and driver bit in the system request because it would have improved processing speeds and memory access times by providing the system identification information for the physical location on the drive from which the data file will be read or written as taught by Jenkins.

7. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723) and further in view of Mizuno et al. (US5,608,891).

As per claim 37, the combination of Anderson and Jones teach the claimed invention as detailed above in the previous paragraphs. However, neither Anderson nor Jones specifically

teach a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device as recited in the claims.

Mizuno discloses a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device [col.17 , lines 8-28].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones and Mizuno before him at the time the invention was made, to modify the system taught by Anderson and Jones to include a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device because it would have improved system performance by reducing the time required for temporarily storing write data in memory and then exclusive oring the data to find redundant data as taught by Mizuno.

Response to Arguments

8. Applicant's arguments filed October 9, 2001 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

The prior art of record does not teach or suggest an interface coupled to a system bus that communicates directly with the BIOS.

Examiner respectfully traverses Applicant's remarks. Examiner would like to point out that the system of Jones comprises a bus interface 108 coupled to a microcontroller CPU 102 with embedded ROM 104 and RAM 106. The ROM contains the firmware for controller 100. There are two distinct areas of firmware. The first one is the Option ROM BIOS, which is contained in the DIP EPROM near the bus connector as detailed in column 23, lines 15-18. It is clearly obvious that the system of Jones provides an interface coupled to a system bus that communicates directly with the BIOS as claimed by Applicant.

Conclusion

9. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c)to consider these references fully when responding to this action. The documents cited therein teach disk striping, bus interface communicating with BIOS, interleave and parallel access to disks.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Monday to Friday 8:30 A.M. to 6:00 P.M., alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are:

After Final (703)746-7238, Non-Official (703)746-7240 and Official (703)746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Matthew M. Kim
Supervisory Patent Examiner

Pierre M. Vital

November 13, 2001